AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method of manufacturing a semiconductor device, the method comprising:

(a) sequentially stacking a first semiconductor layer, a mask layer, and a metal layer on a substrate;

(b) anodizing the metal layer to transform the metal layer into a metal oxide layer including a plurality of nanoholes;

(c) etching the mask layer using the metal oxide layer as an etch mask until the nanoholes are extended to the surface of the first semiconductor layer;

(d) removing the metal oxide layer by etching; and

(e) ~~depositing a second semiconductor layer on the mask layer and the first semiconductor layer~~ forming a second semiconductor layer in and above the mask layer having nanoholes through regrowth of the first semiconductor layer.

~~(f) regrowing said second semiconductor layer present in the mask layer having the nanoholes; and~~

~~wherein in step (f), said second semiconductor layer is regrown until said mask layer is covered by said second semiconductor layer.~~

2. (Original) The method of claim 1, wherein each of the holes has a diameter of about 10 nm to 500 nm.

3. (Original) The method of claim 1, wherein each of the holes occupies less than 50% of the entire area.

4. (Original) The method of claim 1, wherein the mask layer is formed to a thickness of about 50 nm to 500 nm.

5. (Original) The method of claim 1, wherein the first semiconductor layer has a lattice constant which is different from the lattice constant of the substrate.

6. (Original) The method of claim 1, wherein the substrate is formed of one of an inorganic crystal including sapphire, Si, SiC, $MaAl_2O_4$, $NdGaO_3$, $LiGaO_2$, ZnO, or MaO, a III-V group compound semiconductor including GaP or GaAs, and a III group nitride semiconductor including GaN.

7. (Original) The method of claim 1, wherein the first semiconductor layer and the second semiconductor layer are formed of nitride semiconductors.

8. (Original) The method of claim 7, wherein the nitride semiconductor is one of GaN, InGaN, AlGaN, AlInGan, and InGaNAs.

9. (Original) The method of claim 1, wherein the mask layer is formed of one of a polycrystalline semiconductor, a dielectric material, and a metal.

10. (Original) The method of claim 9, wherein the polycrystalline semiconductor layer is one of polysilicon and polycrystalline nitride.

11. (Previously Presented) The method of claim 1, wherein the mask layer is one of silicon oxide, titanium oxide, and zirconium oxide.

12. (Previously Presented) The method of claim 1, wherein the mask layer is a metal that has a melting point of 1200 °C or higher.

13. (Original) The method of claim 12, wherein the metal is one of titanium and tungsten.

14. (Original) The method of claim 1, wherein the metal layer is formed of aluminum.

15. (Original) The method of claim 1, wherein in step (c), the etching process is a dry etch process.

16. (Original) The method of claim 1, wherein in step (e), electrical charge storing material is further deposited in the nanoholes.

17. (Cancelled).

18. (New) The method of claim 1, wherein the second semiconductor layer covers said mask layer.